What is claimed is:

1.A semiconductor device comprising:

a first conductive layer formed of a surface of a semiconductor substrate;

a second conductive layer which is formed close to the first conductive layer, wherein

a distance between the first conductive layer and the second conductive layer is determined in accordance with a permittivity of the insulating layer.

2.A semiconductor device according to claim 1: wherein the second conductive layer is made of a conductive film being filled in

a through hole being located close to said first conductive layer and passing through at least a part of the insulating film; and said first and second conductive layers are connected to first and second potentials, respectively, and a capacitor, which extends in the depth direction of said through hole, is formed by using said insulating inter-layer film interposed between said first conductive layer and said second conductive layer within said through hole.

3.A semiconductor device according to claim 2, wherein said through hole comprises a second through hole being electrically connected to a semiconductor region or a wiring region only at either of the opened ends thereof.

4.A semiconductor device according to claim 2, wherein said through-hole comprises a second through-hole opened to the surface of said insulating region formed on the surface of said substrate.

5.A semiconductor device according to any of claim 2, wherein said through-hole comprises a second through-hole opened to the surface of an element separation region formed on the surface of a semiconductor substrate as said substrate.

6.A semiconductor device according to claim 2, wherein said first conductive layer is formed within a first through-hole being separated by a predetermined distance from said through-hole, whereby a vertical capacitor, which extends in the depth direction of said through-hole, is formed by said first and second conductive layers and said insulating film interposed between said first and second conductive layers.

7.A semiconductor device according to claim 2, wherein said through-hole is rectangular in cross section, and the surface of said through-hole, which is confronted with said first conductive layer, is a wider surface.

8.A semiconductor device according to claim 2, wherein said through-hole comprises a third through-hole opened to the surface of said substrate so as to be electrically connected with the surface of said substrate, and a second through-hole opened to the surface of an insulating region formed on the surface of said substrate, said second and third through-holes

being formed in the same manufacturing step, and the area of the opening of said second through-hole is larger than that of the opening of said third through-hole.

9.A semiconductor device according to claim 6, wherein said through-hole surrounds said first conductive layer while being separated a predetermined distance from the side wall of said first through-hole, and a vertical capacitor, which extends in the depth direction of said through-hole, is formed between the side wall of said first conductive layer and said second conductive layer, which are confronted with each other with said insulating film being interposed therebetween.

10. A semiconductor device according to claim 9, wherein said first conductive layer comprises an insulating protective layer formed on the side wall of said first conductive layer.

11.A semiconductor device according to claim 2, wherein said through-hole overlaps with at least a part of the upper surface of said first conductive layer, and a vertical capacitor, which extends in the depth direction of said through-hole, is formed between the side wall of said first conductive layer and said second conductive layer, which are confronted with each other with said insulating film being interposed therebetween.

12.A semiconductor device according to claim 11, wherein said first conductive layer comprises insulating protective films, which are formed on at least the side wall and the upper

surface of said first conductive layer.

13.A semiconductor device according to claim 12, wherein said through-hole is opened to an areal range from the upper surface to both side walls of said first conductive layer.

14.A semiconductor device according to claim 10, wherein said insulating protective layer consists of a first insulating film and a second insulating film layered on said first insulating layer, said second insulating film having a permittivity smaller than that of said first insulating film and exhibiting etching resistance to the etching conditions of said insulating film.

15.A semiconductor device according to claim 2, wherein said first conductive layer surrounds the outside of said second conductive layer so as to be spaced a predetermined distance from said second conductive layer filled in said through-hole.

16.A semiconductor device according to claim 15, wherein said first conductive layer is formed in formed in a comb shape and said through-holes are formed at the positions sandwiched between the teeth of the comb.

Subd5 17.A semiconductor device according to claim 2, wherein said first and second conductive layers are filled in said first and second through-holes, and the upper ends thereof are connected to said first and second conductive layers, and the spatial intervals in the arrays of said first and second

conductive layers are smaller than those in the arrays of said first and second through-holes.

18. A semiconductor device according to claim 2, wherein said first and second conductive layers are filled in said first and second through-holes, and the upper ends thereof are connected to said first and second conductive layers, and the spatial intervals in the arrays of said first and second through-holes are smaller than those in the arrays of said first and second conductive layers.

19. A semiconductor device according to claim 2, wherein said first and second conductive layers are filled in said first and second through-holes, and the upper ends thereof are connected to said first and second conductive layers, and the spatial intervals in the arrays of said first and second through-holes are substantially equal to those in the arrays of said first and second conductive layers.

20. A semiconductor device according to claim 2, wherein said first conductive layer is a gate electrode wiring, and said second through-hole is a source or drain contact hole, and said second conductive layer is a source or drain wiring.

21. A semiconductor device according to claim 2, wherein said first conductive layer is a gate electrode wiring, and said second through-hole is formed on both sides of said gate electrode wiring on an element isolation region, while being spaced a predetermined distance therefrom.

22.A semiconductor device according to claim 2, wherein said first conductive layer is a gate electrode wiring, and second through-hole is formed along said gate electrode wiring so as to cover said gate electrode wiring of which the surface is covered with an insulating protective film on the element separation region, wherein a vertical capacitor is formed by said gate electrode wiring, said insulating protective film covering said gate electrode wiring, and said second conductive layer within said second through-hole.

23.A semiconductor device according to claim 19, wherein said insulating protective layer is a multi-layer film.

24.A semiconductor device according to claim 2, wherein said second through-hole and said second conductive layer filled therein form a seal ring which is formed surrounding the peripheral edge of the surface of the semiconductor chip, and said first conductive layer is an auxiliary ring formed in said first through-hole in a state that it is spaced a predetermined distance from said seal ring while being arranged parallel to said seal ring, and said seal ring and said auxiliary ring form a vertical capacitor.

25.A semiconductor device according to claim 24, wherein said auxiliary ring is formed so as to electrically contact with said substrate.

26.A semiconductor device according to claim 24, wherein said auxiliary ring is connected with anyone of power source

line and signal line.

27.A method of manufacturing a semiconductor device comprising the steps of:

forming a desired element region in a semiconductor substrate;

forming a wiring layer on the surface of said semiconductor substrate; wherein

said wiring layer forming step comprises

a step of forming a first conductive layer,

a step of forming an insulating inter-layer film,

a step of forming a through-hole by selectively removing said insulating film, and

a step of forming a second conductive layer within said through-hole,

said through-hole forming step comprises a step for simultaneously forming a through-hole for circuit connection and a through-hole for forming a supplemental capacitor in which said first and second conductive layers within said through-hole are located close to each other,

wherein said first and second conductive layers are connected in part to first and second different potentials, thereby forming a capacitor.

28.A method of manufacturing a semiconductor device comprising the steps of:

forming a desired element region in a semiconductor

substrate;

forming a wiring layer on the surface of said semiconductor substrate;

said wiring layer forming step comprises

a step of forming a first conductive layer,

a step of forming an insulating inter-layer film,

a step of forming a through-hole by selectively removing said insulating inter-layer film, and

a step of forming a second conductive layer within said through-hole,

said through-hole forming step comprises a step for simultaneously forming a through-hole for circuit connection and a through-hole for forming a supplemental capacitor in which at least said second conductive layers within said through-hole are located close to each other,

wherein said second conductive layers within said supplemental capacitor are connected to first and second different potentials, thereby forming a supplemental capacitor.

29.A method of manufacturing a semiconductor device according to claim 23, further comprising the steps of:

a step of forming a gate electrode film and a gate electrode layer on the surface of a semiconductor substrate including an element separation region;

a step of forming a source-drain region;

a step of forming an insulating inter-layer film;

a step of forming a through-hole so that said through-hole is opened to said source-drain region by selectively etching said insulating inter-layer film in the vicinity of said electrode layer; and

a step of forming, by forming a conductive layer, a wiring so that said wiring comes in contact with said source and drain regions through said through hole,

said through-hole forming step comprises a step for simultaneously forming said through-hole and another through-hole for a supplemental capacitor at a position located near said gate electrode wiring running on said element separation region,

wherein said wiring and electrode layers are connected to first and second different potentials, respectively, whereby a supplemental capacitor is formed.

30.A method of manufacturing a semiconductor device according to claim 29, wherein said electrode layer forming step comprises a step of covering said gate electrode with an insulating protective film after said gate electrode forming step.

31.A method of manufacturing a semiconductor device comprising the steps of:

forming an insulating inter-layer film on the surface of a substrate including a desired element region;

forming a through-hole by selectively removing a contact hole for electrical connection and said insulating inter-layer film; and

forming a second conductive layer within said through-hole,

said through-hole forming step including a step of forming a plurality of second through-holes while being spaced from one another in order to simultaneously forming a contact region for making an electrical contact and a vertical capacitor,

whereby the adjacent regions of said second conductive layers are respectively connected to first and second potentials, thereby forming a capacitor.